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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,385	08/28/2003	Ruthie D. Lyle	RPS920030137US1	7171

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EXAMINER	
LUGO, DAVID B	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/650,385	LYLE ET AL.	
	Examiner	Art Unit	
	David B. Lugo	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/28/03, 12/11/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 3, 4, 7, 16, 34 and 35 are objected to because of the following informalities:

a. Claim 3, recites "the first" [network] in line 2, however, a "first network" is not previously recited in the claim.

b. Claim 7, line 2, "the interference network" should be --the interfering network--.

c. Claim 16, line 2, "the interference network" should be --the interfering network--.

d. Claim 34, recites "said determining step (b)" in line 1. There is insufficient antecedent basis for this limitation in the claim as step (b) in claim 27 is a "joining" step.

e. Claim 35, line 1, "altering step (c)" should be --altering step (e)--.

Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-26 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 10/650,519 in view of Miller et al. U.S. Patent 7,079,812.

Regarding claims 1 and 11, claims 1 and 8 of the '519 application disclose all of the limitations recited in claims 1 and 11 of the instant application, respectively, except for a processor coupled to a memory which stores code for execution on the processor and which stores network transferable data, where the interference detector and the hop sequencer are coupled to the processor, and the stored network transferable data is transferable over the network.

Miller discloses a processor 140 in a transceiver 30 in Figure 5 which is coupled to a memory 144 which stores instructions for the processor, and coupled to other elements including MAC logic 150 and elements in physical engine 120 which are described as being used to determine signals from interfering networks (col. 4, line 50 to col. 5, line 15), and inherently having stored data that is transferable over the network. Accordingly, it would have been obvious to one of ordinary skill in the art to use a processor coupled to various elements as taught by Miller in the apparatuses of claims 1 and 11 of the instant application in order to control transceiver operation.

Further, claims 1 and 8 of the '519 application include limitations regarding the interference detector and hop sequencer formed on a substrate which are not recited in claims 1 and 11 of the instant application. It would have been obvious to one of ordinary skill in the art to remove those limitations along with their associated functionalities.

Regarding claim 2, it is inherent that the interfering sequence data is attained over the second network in claim 1 of the '519 application.

Regarding claims 3-8 and 12-17 of the instant application, see claims 2-7 and 9-14 of the '519 application, respectively.

Regarding claims 9 and 18, the processor in the combination of respective claims of the '519 application with Miller is considered to control the principal functionality of the apparatus.

Regarding claim 10, the processor in the combination of respective claims of the '519 application with Miller is not disclosed as comprising a plurality of sub-processors. However, it is well known in the art to implement the functions of a processor using a plurality of sub-processors. It would have been obvious to one of ordinary skill in the art to use a plurality of sub-processors as a matter of design consideration.

Regarding claims 20 and 27, claims 1 and 8 of the '519 application disclose all of the limitations recited in claims 1 and 11 of the instant application, respectively, except for the steps performed by a device having a processor and a memory which stores network transferable data. While claims 20 and 27 recite methods and claims 1 and 8 of the '519 application recite apparatuses, one of ordinary skill in the art would recognize that the apparatuses recited in the respective claims of the '519 application can perform the method steps recited in the claims of the instant application, and thus render the method claims obvious.

Miller discloses a processor 140 in a transceiver 30 in Figure 5 which is coupled to a memory 144, and which determines signals from interfering networks (col. 4, line 50 to col. 5, line 15), and inherently having stored data that is transferable over the network. Accordingly, it would have been obvious to one of ordinary skill in the art to use a processor coupled to various

elements as taught by Miller in the apparatuses of claims 1 and 11 of the instant application in order to control transceiver operation.

Further, claims 1 and 8 of the '519 application include limitations regarding the interference detector and hop sequencer formed on a substrate which are not recited in claims 20 and 27 of the instant application. It would have been obvious to one of ordinary skill in the art to remove those limitations along with their associated functionalities.

Regarding claims 21-24 and 28-33 of the instant application, see claims 2-4, 7 and 9-14 of the '519 application, respectively.

Regarding claims 25, 34 and 36, performing the determining step or detecting and joining steps using a slave device is deemed a design consideration.

Regarding claims 26 and 35, performing the altering step using a master device is deemed a design consideration.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 20-23 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Panasik et al. U.S. Patent 6,643,278.

Regarding claim 20, Panasik discloses a method comprising the steps of detecting interference from an interfering network (see Fig. 2, step 22; col. 8, lines 21-35), where Panasik describes that the interfering network may be a FHSS network using a predetermined number of FHSS channels for frequency hopping (col. 10, lines 7-12), determining interference hop sequence data which relates to the first network and making the interference hop sequence data available on the second FHSS network (Fig. 2, step 24; col. 8, lines 36-52; col. 9, line 60 to col. 10, line 2), altering the hop sequence of a second FHSS network based on the interfering hop sequence data (see Fig. 2, steps 30-38; col. 13, lines 6-9; col. 11, lines 1-65), where the altered hop sequence comprises the same number of channels as the predetermined number of channels since the interfering (incumbent) network and the second (newly-entering) network may both be Bluetooth compliant networks (see col. 10, lines 7-12; col. 13, lines 31-34), thus having the same number of predetermined channels, and where the method is performed by a device 40 (Fig. 3) having a processor (44, 46) and a memory (50) which stores network transferable data.

Regarding claim 21, Panasik discloses that the altered hop sequence is a sequence which reduces the frequency of collisions between the networks (col. 6, lines 45-53).

Regarding claim 22, Panasik discloses that the altered hop sequence is the hop sequence of the interfering network having a predetermined translation applied thereto (col. 11, lines 4-7, 53-56).

Regarding claim 23, the altered hop sequence is an offset altered sequence (col. 11, lines 53-59).

Regarding claim 26, Panasik discloses that the method 10 is performed in a newly-formed network, which in a Bluetooth protocol, is formed by a master device.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-10 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panasik et al. in view of Miller et al.

Regarding claim 1, Panasik discloses an apparatus in Figure 3 comprising memory (48, 50), an interference detector (physical engine 44) that detects interference from an interfering network as physical engine 44 is described as performing steps 16-24 of method 10 of Figure 2 (col. 12, lines 36-40) including detecting interference from an interfering network (step 22) and attaining interfering hop sequence data relating to the interfering network (step 24) (see Fig. 2; col. 12, lines 58-62; col. 8, lines 21-52), where Panasik describes that the interfering network may be a FHSS network using a predetermined number of FHSS channels for frequency hopping (col. 10, lines 7-12), and the apparatus further comprises a hop sequencer (MAC controller 46) which alters the hop sequence of a second FHSS network based on the interfering hop sequence data (see Fig. 2, steps 30, 32; col. 13, lines 6-9; col. 11, lines 1-38), where the altered hop sequence comprises the same number of channels as the predetermined number of channels since the interfering (incumbent) network and the second (newly-entering) network may both be Bluetooth compliant networks (see col. 10, lines 7-12; col. 13, lines 31-34), thus having the same number of predetermined channels, and where data stored in memory is transferable over the second network.

Although it is believed to be inherent that the apparatus of Panasik includes a processor, Panasik does not expressly show a processor coupled to the memory, interference detector and hop sequencer. However, it is well known in the art of communications to use a processor in a transceiver to control its operation. For instance, Miller discloses a processor 140 in a transceiver 30 in Figure 5 which is coupled to a memory 144 which stores instructions for the processor, and coupled to other elements including MAC logic 150 and elements in physical engine 120 which are described as being used to determine interferers from networks including interfering Bluetooth networks (col. 4, line 50 to col. 5, line 15). Accordingly, it would have been obvious to one of ordinary skill in the art to use a processor coupled to various elements, as taught by Miller, in the transceiver of Panasik in order to control transceiver operation.

Regarding claim 2, Panasik disclose that the interference detector 44 attains the interfering hop sequence data over the second network (col. 9, line 60 to col. 10, line 2).

Regarding claim 3, Panasik discloses that the altered hop sequence is a sequence which reduces the frequency of collisions between the networks (col. 6, lines 45-53).

Regarding claim 4, Panasik discloses that the altered hop sequence is the hop sequence of the interfering network having a predetermined translation applied thereto (col. 11, lines 4-7, 53-56).

Regarding claim 5, the altered hop sequence is an offset altered sequence (col. 11, lines 53-59).

Regarding claim 6, Panasik discloses in Figure 2 that the hop sequence of the second network is created and modified in steps 30-32, and where an offset is applied thereto in step 38.

Regarding claim 7, Panasik discloses that the offset altered sequence is the hop sequence of the interfering network having an offset applied thereto (col. 11, lines 4-7, 53-56).

Regarding claim 8, Panasik does not disclose that the interference detector detects interference as a degradation in network performance. Miller discloses a system for interference mitigation where traffic statistics indicating degradation in network performance is accumulated and used to detect interference (col. 5, lines 16-30). It would have been obvious to one of ordinary skill in the art to use information regarding degradation in network performance to detect interference as disclosed by Miller, in the system of Panasik because it enables interference detection without continuously searching for interferers.

Regarding claim 9, the processor is considered to control the principal functionality of the apparatus.

Regarding claim 10, Panasik in combination with Miller do not disclose that the processor comprises a plurality of sub-processors. However, it is well known in the art to implement the functions of a processor using a plurality of sub-processors. It would have been obvious to one of ordinary skill in the art to use a plurality of sub-processors to implement the functionality of the processor of Panasik in combination with Miller as a matter of design consideration.

Regarding claim 24, Panasik discloses a method for detecting interference as described above, but does not disclose that interference is detected as a degradation in network performance. Miller discloses a system for interference mitigation where traffic statistics indicating degradation in network performance is accumulated and used to detect interference (col. 5, lines 16-30). It would have been obvious to one of ordinary skill in the art to use

information regarding degradation in network performance to detect interference as disclosed by Miller, in the system of Panasik because it enables interference detection without continuously searching for interferers.

8. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Panasik et al. in view of Kloper et al. U.S. Patent 6,941,110.

Regarding claim 25, Panasik discloses a method for detecting interference as described above, but does not disclose that the step of determining interference hop sequence data is performed by a slave device on a second network.

Kloper discloses a method for mitigating interference with frequency hopping signals by deriving future hop frequencies where a slave device (STA) may be used to detect the interfering frequency hopping signal (col. 4, lines 47-53). It would have been obvious to one of ordinary skill in the art to enable a slave device to detect an interfering signal because the interfering signal may not be affecting the master device but only the slave (e.g. Interfering system 40 – Fig. 1), and accordingly, only the slave device can detect the signal (col. 3, lines 13-15).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David B. Lugo whose telephone number is 571-272-3043. The examiner can normally be reached on M-F; 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

David B. Lugo
Patent Examiner

2/16/07